28-V Low Thermal-Impedance HBT With 20-W CW Output Power

Darrell Hill, *Member, IEEE,* and Tae S. Kim

***Abstract*— AlGaAs/GaAs heterojunction bipolar transistors (HBT's) have been fabricated which exhibit record output power for GaAs flip-chip technology, and record operating voltage for GaAs microwave power devices. Transistors with 2-mm emitter length readily achieved 20-W continuous wave (CW) output power at 2 GHz when biased at 28 V, with typical power-added efficiencies of 62% (typical collector efficiencies of 70%). Maximum CW output power of 25 W was obtained, corresponding to a power density of 12.5 W/mm. All results reported were obtained with devices requiring less than 1-mm^2 die area. High efficiency, high power, and high power density are enabled by the low device temperatures afforded by the thermally efficient low thermal impedance (LTI) technology.**

***Index Terms*— Heterojunction bipolar transistors, microwave bipolar transistors, microwave transistors.**

I. Introduction

GaAs HETEROJUNCTION bipolar transistor (HBT) technology has the potential for providing drop-in replacements for existing silicon bipolar power transistors, delivering much higher power gain and up to twice the RF output power for a given amount of dc power. Such replacement components, if available, would find application in systems where the performance of silicon bipolar transistors is inadequate, such as solid-state transmitters for air-traffic control and other radar systems, and efficient linear-power amplifiers.

The superior power gain of the GaAs HBT, which arises from the heavy base doping (and consequent low base resistance) enabled by the emitter–base heterojunction, is well known. However, the GaAs HBT has other fundamental advantages which will insure superior performance in microwave-power applications even as Si-based heterojunction technologies mature. If a given device geometry and vertical doping profile were implemented in both Si-based and GaAs-based HBT technologies, the resistivity of the lightly doped GaAs collector layer would be less than one-third that of the Si device because of the higher electron mobility of GaAs. The silicon device would, therefore, effectively have additional series resistance on the output. Furthermore, the maximum current density for the GaAs device, as determined by the onset of the Kirk effect, would be roughly double that for the Si device because of the higher effective electron saturated velocity due to the well-established velocity-overshoot phenomenon which arises in GaAs because of band-to-band scattering [1]. Finally, a relatively minor difference would be a slightly higher breakdown voltage for the GaAs device (roughly 10%). Thus, even if these hypothetical silicon and GaAs HBT's had the same power gain under the same operating conditions, the GaAs device could be operated at twice the current density (if thermal effects could be neglected) with significantly lower series resistance on the output. Both the lower resistance and higher maximum current density would contribute to higher collector efficiency (RF output power divided by dc input power) for the GaAs HBT.

Of course, thermal effects may not be neglected for microwave-power transistors. This is especially true for GaAs, which has a thermal conductivity only about one-third that of silicon. In fact, the low thermal conductivity of GaAs underlies two of the three historical obstacles to widespread replacement of silicon power transistors with GaAs HBT's. These obstacles are high cost, relatively low power levels (usually $<$10 W), and relatively low operating voltages (usually $<$10 V). Poor thermal conductivity contributes to both the cost and the low power of GaAs power devices. Comparing again the hypothetical GaAs and silicon HBT's, if the junction temperature is to be equal between the two devices, then clearly the GaAs device must have a significantly lower power dissipation than the silicon device. If the GaAs HBT is nevertheless required to dissipate the same power at the same junction temperature, then the GaAs device must be redesigned to dissipate heat over a significantly larger die. Thus, GaAs power components are expensive not only because of the intrinsically higher cost of GaAs substrates, but also because of larger die sizes due to low thermal conductivity.

The third obstacle—low operating voltage—is not fundamental, but rather historical in nature. The development of HBT technology has been driven by low-voltage, low-power wireless communications applications below 5 GHz, and by military applications at higher frequencies. Because of the fundamental tradeoffs involved, HBT's designed for higher frequencies have also used relatively low operating voltages, typically 10 V or less. However, GaAs HBT's are capable of efficient operation at higher voltages, as was recently demonstrated [2].

In this paper, we report results for an HBT technology which simultaneously addresses the issues of thermal resistance, die size, and operating voltage. By applying low thermal impedance (LTI) technology [3] to HBT structures designed specifically for L/S-band operation, we obtain high-voltage devices with very small die sizes, with thermal resistance dominated by metallization rather than by semiconductor.

Manuscript received March 31, 1997; revised August 15, 1997.

The authors are with Corporate R&D, Texas Instruments Incorporated, Dallas, TX 75265 USA.

Publisher Item Identifier S 0018-9480(97)08324-5.

TABLE I
EPITAXIAL STRUCTURE OF 28-V HBT

Layer	Material	Thickness (nm)	Doping (cm^{-3})
Contact cap	$In_{0.5}Ga_{0.5}As$	30	Si: 1×10^{19}
Grading	InGaAs-GaAs	30	Si: 1×10^{19}
Emitter cap	GaAs	190	Si: 5×10^{18}
Grading	GaAs-AlGaAs	50	Si: 3×10^{17}
Emitter	$Al_{0.35}Ga_{0.65}As$	60	Si: 3×10^{17}
Grading	AlGaAs-GaAs	20	Si: 3×10^{17}
Base	GaAs	800	C: 4×10^{19}
Collector	GaAs	2800	Si: 6×10^{15}
Subcollector	GaAs	500	Si: 5×10^{18}
Buffer	$Al_{0.4}Ga_{0.6}As$	100	Undoped

These devices demonstrate for the first time the feasibility of GaAs HBT's for high-performance drop-in replacements for silicon bipolar power transistors.

II. DEVICE FABRICATION

The HBT epitaxial structure shown in Table I was grown on semi-insulating GaAs by metal–organic chemical vapor deposition. The 2.8-μm-thick collector layer provides a measured base–collector breakdown voltage BV_{CBO} of 70 V.

Basic fabrication (device isolation, formation of ohmic contacts, capacitors, and resistors) was accomplished using a process similar to TI's production HBT process [4]. A large emitter stripe width of 4 μm, together with nonself-aligned base contacts and a depleted emitter ledge structure for surface passivation were used to obtain high yield and reliable operation, although emitter stripes as narrow as 1.2 μm have been fabricated in this technology with high yield. The devices were designed to be unconditionally thermally stable by means of base ballast networks, which have less impact on efficiency than the emitter ballast used by silicon bipolar transistors [5].

Following basic device fabrication, the LTI process was applied to achieve very low thermal resistance. Note that since the LTI process is separate from basic device fabrication, LTI is essentially a device-independent technology, applicable to MESFET's, heterojunction field-effect transistors (HFET's), pseudomorphic high electron-mobility transistors (pHEMT's), and HBT's. For these HBT's, the LTI process began with plating of Au to a thickness of 3 μm to build up the transmission lines and to form air bridges to the emitters. This plated metal also covered most of the wafer surface to provide a microwave ground plane. Nongrounded components (such as base and collector leads) were then covered by a 10-μm-thick polyimide layer. A second plating step was performed to increase the plated Au thickness to 10 μm. The final processing step on the front side of the wafer was sputter deposition of Au to cover the polyimide, providing a low-loss ground plane for the transmission lines embedded in the polyimide. The wafers were then mechanically thinned and polished to achieve a thickness of 100 μm with a specular backside surface suitable for photolithography. After wafer thinning, through-wafer vias were etched and backside plating was performed to obtain electrical connections to the frontside of the wafer.

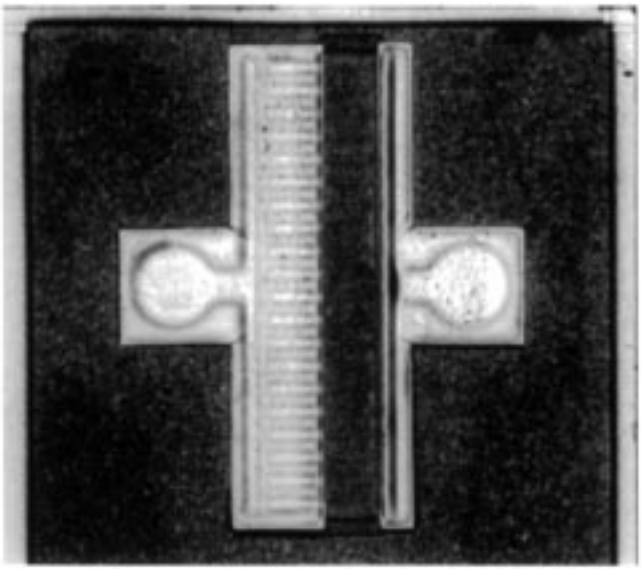

Fig. 1. Active side of 20-W HBT.

For clarity, the side of the chip which contains the transistors is referred to as the "active side," while the other side is referred to as the "passive side." The chip is assembled with the active side against the heat sink for efficient heat removal. Because connections for dc power and RF input/output are made on the passive side of the chip, the flip-chip nature of the die is not detectable without a microscope; no special alignment or flip-chip packaging or assembly is required. In fact, LTI transistors and monolithic microwave integrated circuits (MMIC's) can be designed to provide die which are exact drop-in replacements of die for existing conventional components—except that the LTI components provide higher power densities with lower junction temperatures.

III. RF TESTING

Completed die were mounted on either copper or copper–molybdenum carriers with AuSn solder; no significant differences were seen between devices mounted on copper or copper–molybdenum. Transistors with 2 mm total emitter length were tested at 2 GHz, with external tuning on the input and output to achieve a match to 50 Ω. The output of the device under test was monitored with a spectrum analyzer at all times to insure that no oscillations were present. No tuner or fixture losses were de-embedded, and no intentional harmonic tuning was applied.

The results presented in this paper were obtained with a common-emitter transistor design consisting of 20 emitter fingers in parallel, spaced 40 μm apart; each emitter finger is 4×100 μm^2. The total area required for the transistor, including base ballast network and through-chip vias for contacting the base and collector from the passive side of the chip, is roughly 0.8×0.8 mm^2, or less than 12% of the chip size required for the conventional 30-W HBT we previously reported [2]. The active and passive sides of the chip are shown in Figs. 1 and 2, respectively. More than ten devices from two different epitaxial growth runs have been tested to 20 W at a collector bias of 28 V, with typical associated power-

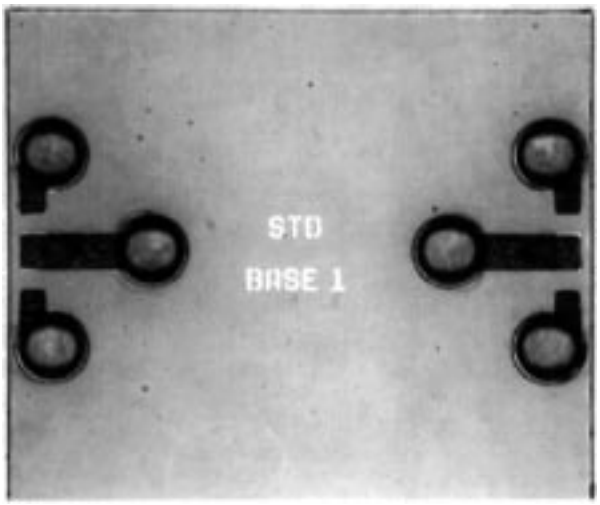

Fig. 2. Passive side of 20-W HBT.

added efficiency (PAE) of 62% (typical collector efficiency of 70%). The highest PAE measured at 20 W continuous wave (CW) output power at 2 GHz was 64.4% PAE (70.7% collector efficiency) with 11.1-dB associated gain under class-B operation (zero quiescent current). This was achieved at 28 V, with 1.01-A collector current. When tuned for maximum gain under class-B operation, power gain of 15 dB was obtained (power gain under linear class-A operation was not measured, but would be expected to be several decibels higher).

Output power of 20-W CW at 28 V is the nominal operating point for these devices. However, transistors of this design have been operated to 25-W CW output power, and bias levels up to 31.5 V. At 25-W output power, the collector current was 1.36 A at $V_{\rm CE} = 28$ V, so that collector efficiency was over 65%; however, power gain dropped to 7 dB, so that PAE was somewhat lower at 52.6%.

IV. Thermal Performance

The ability to deliver high power from such a small die is due not only to the low thermal resistance of the LTI configuration, but also to the high PAE. The power dissipated within the device at the 20-W operating condition is

$$\begin{aligned} P_{\rm DISS} &= P_{\rm dc} + P_{\rm IN} - P_{\rm OUT} \\ &= [V_{\rm CE}I_C + V_{\rm BE}I_B] + P_{\rm IN} - P_{\rm OUT} \\ &= [28\ \text{V}(1.01\ \text{A}) + 0.7\ \text{V}(0.024\ \text{A})] + 1.6\ \text{W} - 20\ \text{W} \\ &= 9.9\text{W}. \end{aligned}$$

Thermal resistance of this device is 10 °C/W, as predicted by thermal modeling and confirmed by infrared scan (described below). The maximum junction temperature rise, therefore, is only about 100 °C above baseplate at 20-W CW output power. The success of the LTI configuration is perhaps best indicated by the fact that according to thermal modeling, only 25% of the total thermal resistance (2.5 °C/W) is due to semiconductor. A much greater temperature drop—roughly 50%—occurs across the plated Au metallization, with the remainder across the solder used to attach the chip to the heatsink. This seems to imply that emerging technologies such as SiC and diamond may require novel packaging strategies to maintain a decisive advantage in terms of thermal resistance.

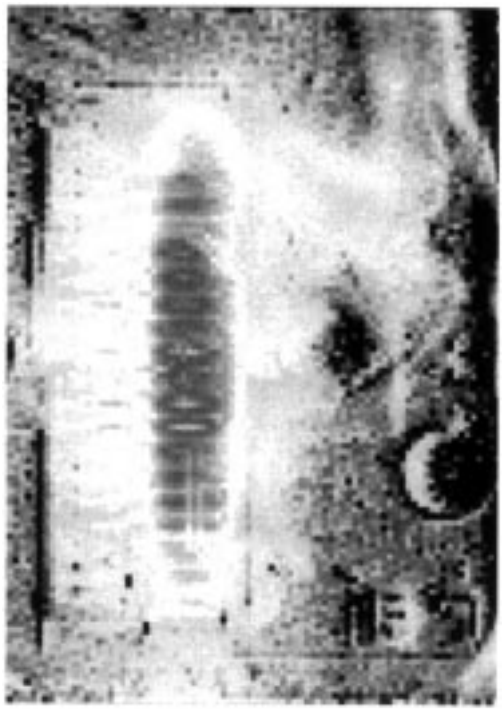

Fig. 3. IR scan of LTI HBT (emitter fingers on bottom (active side) of chip are clearly visible).

Infrared (IR) scans were performed on assembled devices using a Barnes Engineering IR system with a detector sensitive to wavelengths from 1.5 to 5.5 μm. Over this wavelength range, GaAs is quite transparent, enabling straightforward imaging of individual emitter fingers even though the die was mounted inverted. Fig. 3 shows an IR scan of a device at a power dissipation of 4 W; emitters and other features on the active side of the die are clearly visible. These features vanish when the chip is coated with a thin layer of black paint (Fig. 4).

For the IR scan, the same fixtures used for RF testing were individually bolted to a hot plate set at 60 °C, with a thermocouple inserted into the base of the fixture under test to monitor baseplate temperature. Different levels of power dissipation were achieved by varying the collector voltage and current. At each power dissipation level, the maximum temperature seen anywhere in the device was recorded. As might be expected, maximum temperature occurred near the center of the central fingers, indicating that thermal resistance can be reduced further by techniques such as nonuniform finger spacing. The maximum temperature is plotted as a function of power dissipation to determine the thermal resistance of the device, with the results shown in Fig. 5. We attribute the somewhat higher value of thermal resistance at the lowest power dissipation to noise in the temperature measurement at this dissipation due to the low associated temperature rise (10.6 °C). The slight slope seen at higher dissipation levels is expected because of the nonconstant thermal conductivity of GaAs over temperature. At a baseplate temperature of 60 °C, the thermal resistance is found to be near 10 °C/W over

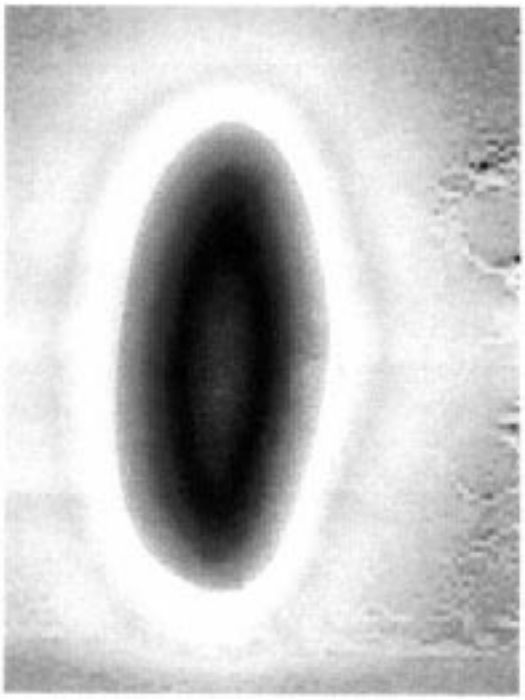

Fig. 4. IR scan of LTI HBT with a thin layer of black paint (no temperature variations related to individual emitter fingers are visible).

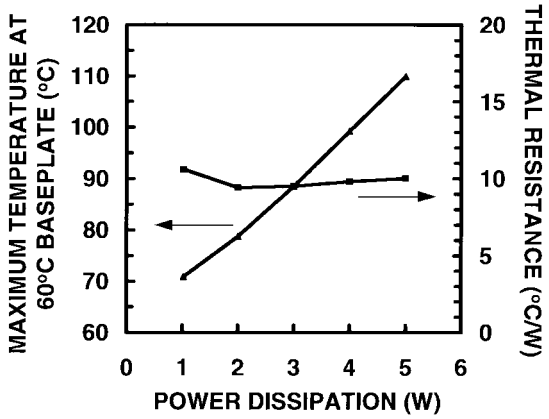

Fig. 5. Temperature and thermal resistance as a function of power dissipation at 60 °C baseplate.

junction temperatures from 70 °C to 110 °C, in agreement with thermal modeling.

Despite the high power density, these devices are not particularly sensitive to variations in baseplate temperature. As shown in Fig. 6, CW output power dropped only 0.3 dB from 15.8 W (42 dBm) at 0 °C to 14.8 W (41.7 dBm) at 60 °C baseplate temperature, while PAE dropped from 64% to 61.7% (collector efficiency from 71.4% to 69.4%).

V. Discussion

To our knowledge, the results presented in this paper represent state-of-the-art performance for CW power transistors in this frequency range, despite the fact that they were obtained with a first-pass unit cell design. Improvements to the cell design, the use of harmonic tuning, and pulsed operation may result in substantially higher efficiency and peak output power. However, even without such changes, the power gain of these first-pass devices is sufficiently high that straightforward power-combining of these compact cells should result in single-chip power levels which are unprecedented for GaAs microwave devices.

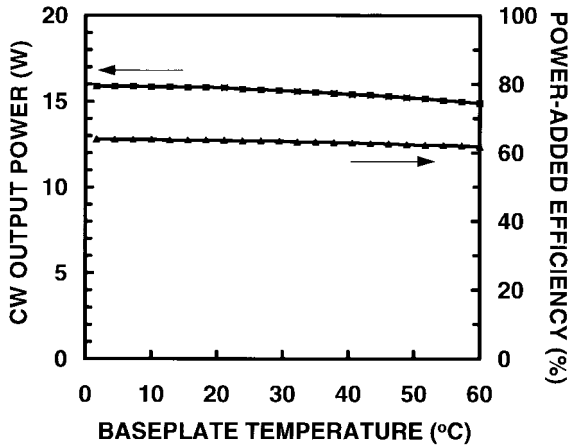

Fig. 6. Output power and PAE versus baseplate temperature.

Although 20-W operation corresponds to a high power density of 10 W/mm, the record operating voltage and wide emitter stripe allowed for a relatively low emitter current density of 12.6 kA/cm^2. Low current density is important for long-term reliability, since HBT median time to failure is inversely proportional to the square of current density [6], [7]. Because thermal resistance is dominated by metallization rather than semiconductor in these devices, the maximum junction temperature rise of 100 °C is actually rather low compared to many commercially available silicon-power transistors. For applications where even lower junction temperature is required, we have demonstrated that these devices may be operated at reduced power levels of 10–15 W with little or no degradation of efficiency and with somewhat higher power gain. For example, the device which achieved 64.4% PAE at 20 W also had 64.4% PAE at 15 W, with 12.9 dB gain; backed off even further to 10 W, the device achieved 57% PAE with 13.8 dB gain.

As might be expected, the per-wafer cost of LTI device processing (for FET's, pHEMT's, or HBT's) is somewhat higher than for conventional versions of the same devices because of the additional processing steps. Nevertheless, the cost per watt should be lower than for non-LTI technologies in GaAs because of LTI's capability for dramatically higher power density—particularly for HBT's. Compared to 5.3 W/mm^2 (*saturated* output power per unit area of GaAs die) for a high-performance power FET using 1.6-mil GaAs [8], the demonstrated *nominal* power density of $>$31 W/mm^2 using 4-mil GaAs gives the LTI technology a considerable advantage in die size.

VI. Conclusion

HBT's fabricated using LTI technology have demonstrated record operating voltage for GaAs microwave devices, and state-of-the-art performance for CW power transistors at

S-band. At 2 GHz, a common-emitter HBT biased at 28 V delivered 20-W CW output power with 11.1-dB gain and 64.4% PAE (collector efficiency of 70.7%) under class-B operation. Despite use of a very compact device occupying roughly 0.8×0.8 mm^2, the maximum junction temperature rise was only 100 °C above baseplate. The ability to fabricate high-performance GaAs HBT's with operating voltages compatible with existing silicon bipolar power devices should allow relatively straightforward upgrades of existing systems. The demonstrated power/efficiency performance should also be attractive for emerging applications with stringent requirements on volume and cooling, such as compact base stations for wireless communications.

ACKNOWLEDGMENT

The authors would like to acknowledge the technical assistance of G. Ross, W. Johnson, J. Hartsell, B. Smith, and D. McManaman.

REFERENCES

[1] R. Katoh, M. Kurata, and J. Yoshida, "Self-consistent particle simulation for (AlGa)As/GaAs HBT's with improved base–collector structures," *IEEE Trans. Electron Devices*, vol. 36, pp. 846–853, May 1989.

[2] D. Hill, H. Q. Tserng, T. Kim, and M. Tutt, "Single-chip 30 W CW AlGaAs/GaAs heterojunction bipolar transistor at 3 GHz," in *Proc. GaAs IC Symp. Dig.*, Orlando, FL, Nov. 1996, pp. 229–232.

[3] D. Hill, R. Yarborough, T. Kim, and H.-F. Chau, "Low thermal impedance MMIC technology," *IEEE Microwave Guided Wave Lett.*, vol. 7, pp. 36–38, Feb. 1997.

[4] W. Liu, S. Nelson, D. G. Hill, and A. Khatibzadeh, "Current gain collapse in microwave multifinger heterojunction bipolar transistors operated at very high power densities," *IEEE Trans. Electron Devices*, vol. 40, pp. 1917–1927, Nov. 1993.

[5] W. Liu, A. Khatibzadeh, J. Sweder, and H.-F. Chau, "The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 245–251, Feb. 1996.

[6] H. Sugahara, J. Nagano, T. Nittono, and K. Ogawa, "Improved reliability of AlGaAs/GaAs heterojunction bipolar transistors with a strain-relaxed base," in *Proc. GaAs IC Symp. Dig.*, San Jose, CA, Oct. 1993, pp. 115–118.

[7] T. Henderson, "Model for degradation of GaAs/AlGaAs HBT's under temperature and current stress," *IEDM Tech. Dig.*, pp. 811–814, 1995.

[8] H. Ishimura, M. Murayama, K. Arai, Y. Saito, Y. Oda, and H. Kuroda, "L- and S-band 50-W power GaAs MESFET's," in *IEEE MTT-S Dig.*, San Francisco, CA, June 1996, pp. 539–542.

Darrell Hill (M'92) received the B.S. degree in electrical engineering from Rice University, Houston, TX, in 1983, and the M.S. and Ph.D. from Stanford University, Stanford, CA, in 1985 and 1990, respectively.

In 1990, he joined Texas Instruments Incorporated, Dallas, TX, where he was initially involved in the development of a high-performance monolithic complementary HBT technology. His work has also focused on HBT's for microwave-power applications, including providing the first explanation of the thermal-collapse phenomenon seen in unballasted HBT's. He is currently responsible for development of HBT's with high-voltage operation, low thermal-impedance devices with high power and power density, and high-performance HBT's at 20 GHz. He has authored or co-authored over 20 HBT-related papers and holds over a dozen U.S. patents.

Tae S. Kim received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1979, and the Ph.D. degree in electrical engineering from the University of Texas at Austin, in 1981, and 1987, respectively.

In 1987, he joined Texas Instruments Incorporated, Dallas, TX, where he has worked on characterization, ion implantation, and epitaxy of III–V compound semiconductors.